JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

SEMESTER – I

S. No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D06101	Digital System Design with PLDs	PC	3	0	0	3
2.	21D06102	Microcontrollers and Programmable Digital Signal Processors	PC	3	0	0	3
3.	21D06103a 21D06103b 21D06103c	**Program Elective – I** Advanced Computer Architecture Design of Fault Tolerant Systems Advanced Operating System	PE	3	0	0	3
4.	21D06104a 21D06104b 21D06104c	**Program Elective – II** CMOS Digital IC Design Digital Signal Processors and Architectures Advanced Data Communication	PE	3	0	0	3
5.	21D06105	Digital System Design Lab	PC	0	0	4	2
6.	21D06106	Microcontrollers and Programmable Digital Signal Processors Lab	PC	0	0	4	2
7.	21DRM101	Research Methodology and IPR	MC	2	0	0	2
8.	21DAC101a 21DAC101b 21DAC101c	**Audit Course – I** English for Research paper writing Disaster Management Sanskrit for Technical Knowledge	AC	2	0	0	0
		Total					**18**

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SEMESTER – II

S.No.	Course codes	Course Name	Category	Hours per			Credits
				L	T	P	
1.	21D06201	Embedded System Design	PC	3	0	0	3
2.	21D06202	VLSI Technology and Design	PC	3	0	0	3
3.	21D06203a 21D06203b 21D06203c	**Program Elective – III** SoC Architecture Embedded Software Engineering Embedded Real Time Operating Systems	PE	3	0	0	3
4.	21D06204a 21D06204b 21D06204c	**Program Elective – IV** Hardware and Software co-design Adhoc and Wireless Sensor Networks Algorithms for VLSI Design	PE	3	0	0	3
5.	21D06205	Embedded System Design Lab	PC	0	0	4	2
6.	21D06206	VLSI Simulation Lab	PC	0	0	4	2
7.	21D06207	Technical seminar	PR	0	0	4	2
8.	21DAC201a 21DAC201b 21DAC201c	**Audit Course – II** Pedagogy Studies Stress Management for Yoga Personality Development through Life Enlightenment Skills	AC	2	0	0	0
Total							**18**

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SEMSTER - III

S.No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D06301a 21D06301b 21D06301c	**Program Elective – V** Embedded Systems Protocols Soft Computing Techniques Communication Buses and Interfaces	PE	3	0	0	3
2.	21DOE301b 21DOE301c 21DOE301e	**Open Elective** Industrial Safety Business Analytics Waste to Energy	OE	3	0	0	3
3.	21D06303	Dissertation Phase – I	PR	0	0	20	10
4.	21D06304	Co-curricular Activities					2
Total							**18**

SEMESTER - IV

S.No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D06401	Dissertation Phase – II	PR	0	0	32	16
Total							**16**

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COURSE STRUCTURE & SYLLABI

Course Code	DIGITAL SYSTEM DESIGN with PLDs	L	T	P	C
21D06101		3	0	0	3
	Semester	I			

Course Objectives:

- To understand an overview of system design approach using programmable logic devices.
- To get exposed to the various architectural features of CPLDS and FPGAS.
- To learn the methods and techniques of CPLD & FPGA design with EDA tools.
- To learn software tools used for design process with the help of case studies.

Course Outcomes (CO): Student will be able to

- Understand an overview of system design approach using programmable logic devices.
- Get exposed to the various architectural features of CPLDS and FPGAS.
- Learn the methods and techniques of CPLD & FPGA design with EDA tools.
- Learn software tools used for design process with the help of case studies.

UNIT - I Lecture Hrs:

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, CLB and slice Stratix LAB and ALM-RAM Blocks, Different types Xilinx FPGAs, DSP Blocks, Clock Management, I/O standards, Additional features.

UNIT - II Lecture Hrs:

Analysis and Derivation of Clocked Sequential Circuits with State Graphs and Tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation

UNIT - III Lecture Hrs:

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design

UNIT - IV Lecture Hrs:

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults.

UNIT - V Lecture Hrs:

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Textbooks:

1.Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Logic Design Theory-N.N.Biswas,PHI.

Reference Books:

1. Digital Circuits and Logic Design-Samuel C.LEE,PHI, 2008.
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.

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COURSE STRUCTURE & SYLLABI

Course Code	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS	L	T	P	C
21D06102		3	0	0	3
	Semester	I			

Course Objectives:

- To learn about ARM Microcontroller architectural features
- To understand the ARM 'C' Programming for various applications
- To study the DSP processor fundamentals and its development tools

Course Outcomes (CO): Student will be able to

- Learn about ARM Microcontroller architectural features
- Understand the ARM 'C' Programming for various applications
- Study the DSP processor fundamentals and its development tools

UNIT - I	Lecture Hrs:

ARM Cortex-Mx Processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence, Instruction Set (ARM and Thumb), Unified AssemblerLanguage, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT - II	Lecture Hrs:

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT - III	Lecture Hrs:

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT - IV	Lecture Hrs:

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT - V	Lecture Hrs:

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Textbooks:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH, 2nd Edition.

Reference Books:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

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COURSE STRUCTURE & SYLLABI

Course Code	ADVANCED COMPUTER ARCHITECTURES	L	T	P	C
21D06103a	Program Elective – I	3	0	0	3
	Semester	I			

Course Objectives:

- To learn the instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
- To understand the advanced concepts such as instruction level parallelism, , out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.
- To study the multiprocessor and parallel processing architectures.
- To learn about the organization and design of contemporary processor architectures.

Course Outcomes (CO): Student will be able to

- Learn the instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
- Understand the advanced concepts such as instruction level parallelism, out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.
- Study the multiprocessor and parallel processing architectures.
- Learn about the organization and design of contemporary processor architectures.

UNIT - I		Lecture Hrs:

Fundamentals of Computer Design
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II		Lecture Hrs:

Pipelines
Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design
Introduction, review of fundamentals of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - III		Lecture Hrs:

Instruction Level Parallelism the Hardware Approach
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach
Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV		Lecture Hrs:

Multi Processors and Thread Level Parallelism
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT - V		Lecture Hrs:

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COURSE STRUCTURE & SYLLABI

Inter Connection and Networks Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. **Intel Architecture** Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.
Textbooks:
1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.
Reference Books:
1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors 2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill., 3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain, Peter Kacsuk ,Pearson Ed.,

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COURSE STRUCTURE & SYLLABI

Course Code	DESIGN OF FAULT TOLERANT SYSTEMS	L	T	P	C
21D06103b	Program Elective – I	3	0	0	3
	Semester	I			

Course Objectives:

- To provide broad understanding of fault diagnosis and tolerant design approach.
- To illustrate the framework of test pattern generation using semi and full automatic approach.
- To acquire the knowledge of scan architectures.
- To acquire the knowledge of design of built-in-self test.

Course Outcomes (CO): Student will be able to

- Provide broad understanding of fault diagnosis and tolerant design approach.
- Illustrate the framework of test pattern generation using semi and full automatic approach.
- Acquire the knowledge of scan architectures.
- Acquire the knowledge of design of built-in-self test.

UNIT - I Lecture Hrs:

Fault Tolerant Design
Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design
Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT - II Lecture Hrs:

Self Checking circuits & Fail safe Design
Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
Fail Safe Design- Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design

UNIT - III Lecture Hrs:

Design for Testability
Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.
Design for testability by means of scan
Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT - IV Lecture Hrs:

Logic Built-in-self-test
BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

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COURSE STRUCTURE & SYLLABI

UNIT - V		Lecture Hrs:
Standard IEEE Test Access Methods Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.		
Textbooks:		
1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala,PHI, 1984. 2. Digital System Test and Testable Design using HDL models and Architectures - ZainalabedinNavabi, Springer International Ed.,		
Reference Books:		
1. Digital Systems Testing and Testable Design-MironAbramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books 2. Essentials of Electronic Testing- Bushnell &VishwaniD.Agarwal,Springers. 3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008		

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COURSE STRUCTURE & SYLLABI

Course Code	ADVANCED OPERATING SYSTEMS	L	T	P	C
21D06103c	Program Elective – I	3	0	0	3
	Semester	I			

Course Objectives:

- To understand the basics of operating systems
- To learn the features of UNIX and LINUX
- To understand the concepts of distributed systems

Course Outcomes (CO): Student will be able to

- Understand the basics of operating systems
- Learn the features of UNIX and LINUX
- Understand the concepts of distributed systems

UNIT - I		Lecture Hrs:

Introduction to Operating Systems
Overview of computer system hardware, Instruction execution, I/O function, |Interrupts, Memory hierarchy, I/O communication techniques, Operating system objectives and functions, Evaluation of operating system.

UNIT - II		Lecture Hrs:

Introduction to UNIX and LINUX
Basic commands & command arguments, standard input, output, input / output redirection, filters and editors, Shells and operations.

UNIT - III		Lecture Hrs:

System Calls
System calls and related file structures, input / output Process creation & termination.
Inter Process Communication
Introduction, file and record locking, Client-Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT - IV		Lecture Hrs:

Introduction to Distributed Systems
Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed Systems
Layered protocols, ATM networks, Client – Server model, Remote procedure call and Group communication.

UNIT - V		Lecture Hrs:

Synchronization in Distributed Systems
Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions.
Deadlocks
Deadlock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

Textbooks:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, PHI, 1986.
2 Distributed Operating System – Andrew. S. Tanenbaum, PHI, 1994.
3.The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw-Hill.

Reference Books:

1. Operating Systems: Internal and Design Principles – Stallings, 6th Ed., PE.
2.Modern operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.

3.Operating System Principles' – Abraham Silberchatz, peter B. Galvin, Greg Gagne,7th Ed., John Wiley.
4.UNIX User Guide – Ritchie & Yates.
5UNIX Network Programming – W. Richard Stevens, PHI, 1998

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COURSE STRUCTURE & SYLLABI

Course Code	CMOS DIGITAL IC DESIGN	L	T	P	C
21D06104a	Program Elective – II	3	0	0	3
	Semester	I			

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes (CO): Student will be able to

- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
- Estimate Delay and Power of Adders circuits.
- Classify different semiconductor memories.
- Analyze, design and implement combinational and sequential MOS logic circuits.
- Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area of digital ICs

UNIT - I — Lecture Hrs:

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT - II — Lecture Hrs:

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT - III — Lecture Hrs:

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT - IV — Lecture Hrs:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT - V — Lecture Hrs:

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

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COURSE STRUCTURE & SYLLABI

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

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COURSE STRUCTURE & SYLLABI

Course Code	DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES Program Elective – II	L	T	P	C
21D06104b		3	0	0	3
	Semester	I			

Course Objectives:

- To provide a comprehensive understanding of various programs of Digital Signal Processors.
- To distinguish between the architectural differences of ARM and DSPs along with floating point capabilities.
- To explore architecture and functionality of various DSP Processors and can able to write programs.
  To know about the connectivity of interfacing devices with processors

Course Outcomes (CO):

- Provide a comprehensive understanding of various programs of Digital Signal Processors.
- Distinguish between the architectural differences of ARM and DSPs along with floating point capabilities.
- Explore architecture and functionality of various DSP Processors and can able to write programs.
- Know about the connectivity of interfacing devices with processors.

UNIT - I — Lecture Hrs:

Fundamentals of Digital Signal Processing
Digital signal-processing system, Sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and Interpolation, Computational Accuracy in DSP Implementations- Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT - II — Lecture Hrs:

Architectures for Programmable DSP Devices
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT - III — Lecture Hrs:

Programmable Digital Signal Processors
Commercial Digital Signal-Processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX Processors.

UNIT - IV — Lecture Hrs:

Analog Devices Family of DSP Devices
Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to BlackfinProcessor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals

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COURSE STRUCTURE & SYLLABI

UNIT - V		Lecture Hrs:
Interfacing Memory and I/O Peripherals to Programmable DSP Devices Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).		
Textbooks:		
1. Digital Signal Processing: Principles, Algorithms & Applications – J.G. Proakis& D.G. Manolakis, 4th Ed., PHI,2006. 2.Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.		
Reference Books:		
1. A Practical Approach to Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2009. 2. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, TMH, 2002. 3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al., S. Chand & Co. 2000.		

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COURSE STRUCTURE & SYLLABI

Course Code	ADVANCED DATA COMMUNICATIONS	L	T	P	C
21D06104c	Program Elective – II	3	0	0	3
	Semester	I			

Course Objectives:

- To learn about basics of Data Communication networks, different protocols, standards and layering concepts.
- To study about error detection and correction techniques.
- To know about link layer, point to point, Medium Access and Control sub layer protocols.
- To know about Switching circuits, Multiplexing and Spectrum Spreading techniques for data transmission.

Course Outcomes (CO):

- Understand the concepts of Networks and data link layer.
- Acquire the knowledge of error detection, forward and reverse error correction techniques.
- Compare the performance of different MAC protocols like Aloha, CSMA, CSMA/CA, TDMA, FDMA & CDMA.
- Understand the significance of Switching circuits and characteristics of Wired LANs

UNIT - I — Lecture Hrs:

Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface.

Data Link Layer

Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

UNIT - II — Lecture Hrs:

Error Detection and Correction

Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks, Error Correction, Error correction single bit, Hamming code.

Cyclic Codes

Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum

Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol

UNIT - III — Lecture Hrs:

Media Access Control (MAC) Sub Layer

Random Access, ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA),Controlled Access- Reservation, Polling- Token Passing, Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).

Wired LANS

Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet

UNIT - IV — Lecture Hrs:

Switching

Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch

Multiplexing

Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing.

Spectrum Spreading Spread Spectrum-Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum **Connecting devices** Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.		
UNIT - V		Lecture Hrs:
Networks Layer Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches. **Unicast Routing** Introduction, Routing Algorithms-Distance Vector Routing, Link State Routing, Path Vector Routing, Unicast Routing Protocols- Routing Information Protocol(RIP), Open Short Path First .		
Textbooks:		
1. Data Communications and Networking - B. A. Forouzan, 5th Ed., TMH, 2013. 2.Data and Computer Communications - William Stallings, 8th Ed., PHI, 2007.		
Reference Books:		
1. Data Communications and Computer Networks - Prakash C. Gupta, PHI, 2006. 2.Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2008		

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M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

Course Code	DIGITAL SYSTEM DESIGN LAB	L	T	P	C
21D06105		0	0	4	2
	Semester	I			

Course Objectives:

- To familiarize the HDL simulator / synthesis tool
- To design and implement given combinational circuit on FPGA device
- To design and implement given sequential circuit on FPGA device

Course Outcomes (CO):

- Familiarize the HDL simulator / synthesis tool
- Design and implement given combinational circuit on FPGA device
- Design and implement given sequential circuit on FPGA device

List of Experiments:

Student has to design his/her user defined library components by using and standard HDL simulator / Synthesis tool for target FPGA device.

1. Combinational Logic Circuits
   a. Generic Multiplexer.
   b. Generic Priority Encoder.
   c. Design of RAM Memory.
   d. Code Converters.
   e. Combinational Arithmetic circuits
   f. Ripple Carry Adder.
   g. Carry-Look ahead adder.
   h. Signed and Unsigned Adders.
   i. Signed and Unsigned Subtractors.
   j. N-bit Comparator.
   k. N – bit Arithmetic Logic Unit.
   l. Parallel Signed and unsigned Multipliers.
   m. Dividers.
2. Sequential Circuits
   a. Shift Register with Load.
   b. Switch Debouncer.
   c. Timer.
   d. Fibonacci Series Generator.
   e. Frequency Meters.

Software Requirements:
Xilinx Vivado, Intel Quartus Prime Pro, Lattice Diamond, equivalent EDA software
Hardware Requirements:
Xilinx / Altera / Lattice / Equivalent FPGA development kits

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M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

Course Code	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB	L	T	P	C
21D06106		0	0	4	2
	Semester	I			

Course Objectives:

- To write the ARM 'C' programming for applications
- To understand the interfacing of various modules with ARM 7/ ARM Cortex-M3
- To develop assembly and C Programming for DSP processors

Course Outcomes (CO):

- Install, configure and utilize tool sets for developing applications based on ARM processor core.
- Design and developtheARM7 based embedded systems for various applications.
- Develop application programs on ARM and DSP development boards both in assembly and C.
- Design and Implement the digital filters on DSP6713 processor.
- Analyze the hardware and software interaction and integration.

List of Experiments:

Part A) Experiments to be carried out on Cortex-Mx development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

12. To develop an assembly code and C code to compute Euclidian distance between any two points
13. To develop assembly code and study the impact of parallel, serial and mixed execution
14. To develop assembly and C code for implementation of convolution operation
15. To design and implement filters in C to enhance the features of given input sequence/signa

Software Requirements:
Keil for ARM, Code Composer Studio
Hardware Requirements:
ARM Cortex Mx Development Boards, TI TMS C6713 evaluation kit

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COURSE STRUCTURE & SYLLABI

Course Code	RESEARCH METHODOLOGY AND IPR	L	T	P	C
21DRM101		2	0	0	2
	Semester	I			

Course Objectives:

- Identify an appropriate research problem in their interesting domain.
- Understand ethical issues understand the Preparation of a research project thesis report.
- Understand the Preparation of a research project thesis report
- Understand the law of patent and copyrights.
- Understand the Adequate knowledge on IPR

Course Outcomes (CO): Student will be able to

- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT - I Lecture Hrs:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT - II Lecture Hrs:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT - III Lecture Hrs:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - IV Lecture Hrs:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT - V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

Reference Books:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.

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5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.

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M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEMS DESIGN	L	T	P	C
21D06201		3	0	0	3
	Semester	**II**			

Course Objectives:

- To differentiate between a General purpose and an Embedded System.
- To provide knowledge on the building blocks of Embedded System.
- To understand the requirement of Embedded firmware and its role in API.

Course Outcomes (CO): Student will be able to

- Expected to differentiate the design requirements between General Purpose and Embedded Systems.
- Expected to acquire the knowledge of firmware design principles.
- Expected to understand the role of Real Time Operating System in Embedded Design.
- To acquire the knowledge and experience of task level Communication in any Embedded System.

UNIT - I	Lecture Hrs:
Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.	
UNIT - II	Lecture Hrs:
Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces. DDR , Flash, NVRAM	
UNIT - III	Lecture Hrs:
Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.	
UNIT - IV	Lecture Hrs:
RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.	
UNIT - V	Lecture Hrs:
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.	

Textbooks:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

Reference Books:

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

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M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

Course Code	VLSI TECHNOLOGY AND DESIGN	L	T	P	C
21D06202		3	0	0	3
	Semester	**II**			

Course Objectives:

- To familiarize with large scale integration technology.
- To expose fabrication methods, layout and design rules.
- To learn methods to improve Digital VLSI system's performance.
- To know about VLSI Design constraints.

Course Outcomes (CO):

- Familiarize with large scale integration technology.
- Expose fabrication methods, layout and design rules.
- Learn methods to improve Digital VLSI system's performance.
- Know about VLSI Design constraints.

UNIT - I	Lecture Hrs:

Review of Microelectronics and Introduction to MOS Technologies-
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage V_T, g_m, g_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT - II	Lecture Hrs:

Layout Design and Tools
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT - III	Lecture Hrs:

Combinational Logic Networks
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT - IV	Lecture Hrs:

Sequential Systems
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT - V	Lecture Hrs:

Floor Planning
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Essentials of VLSI Circuits and Systems, K. EshraghianEshraghian. D, A. Pucknell, 2005, PHI.
3. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

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M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

Course Code	SoC ARCHITECTURE	L	T	P	C
21D06203a	Program Elective – III	3	0	0	3
	Semester	II			

Course Objectives:

- To understand the basics related to SoC architecture and different approaches related to SoC Design.
- To select an appropriate robust processor for SoC Design
- To select an appropriate memory for SoC Design.
- To realize real time case studies

Course Outcomes (CO): Student will be able to

- Understand the basics related to SoC architecture and different approaches related to SoC Design.
- Select an appropriated robust processor for SoC Design
- Select an appropriate memory for SoC Design.
- Realize real time case studies

UNIT - I		Lecture Hrs:

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT - II		Lecture Hrs:

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT - III		Lecture Hrs:

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV		Lecture Hrs:

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT - V		Lecture Hrs:

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

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COURSE STRUCTURE & SYLLABI

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2.Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.
3.System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers

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COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SOFTWARE ENGINEERING	L	T	P	C
21D06203b	Program Elective – III	3	0	0	3
	Semester	II			

Course Objectives:

- To familiarize about embedded and real-time systems
- To learn about embedded software build process
- To learn embedded programming and operating system concept

Course Outcomes (CO):

- Familiarize about embedded and real-time systems
- Learn about embedded software build process
- Learn embedded programming and operating system concepts

UNIT - I — Lecture Hrs:

Software Engineering of Embedded and Real-Time Systems
Software engineering, Embedded systems, Embedded systems are reactive systems, Real-time systems, Soft and Hard Real-Time systems, Efficient execution and the execution environment, Resource management, Challenges in real-time system design.

UNIT - II — Lecture Hrs:

The embedded system software build process, Distributed and multi-processor architectures, Software for embedded systems, Super loop architecture, Power-save super loop, Window lift embedded design, Hardware abstraction layers (HAL) for embedded systems, HW/SW prototyping, Industry design chain, Different types of virtual prototypes, Architecture virtual prototypes, Software virtual prototypes.

UNIT - III — Lecture Hrs:

Events, Triggers and Hardware Interface to Embedded Software
Events and triggers, Event system, Event handle, Event methods, Event data structure, Reentrancy, Disable and enable interrupts, Semaphores, Implementation with Enter/ExitCritical, Event processing, Integration, Triggers, Blinking LED, Design idea, Tick timer, Trigger interface, Trigger descriptor, Data allocation, SetTrigger, IncTicks, Making it reentrant, Initialization, Real-time aspects, Introduction to Hardware Interface, Collaboration, System integration, Launching tasks in hardware, Debug hooks, Compile-time switches, Build-time switches, Run-time switches, Self-adapting switches, Difficult hardware interactions, Testing and troubleshooting.

UNIT - IV — Lecture Hrs:

Embedded Software Programming and Operating Systems
Introduction, Principles of high-quality programming, Readability, Maintainability, Testability, Starting the embedded software project, Libraries from third parties, Team programming guidelines, Syntax standard, Conditional compilation, Foreground/background systems, Real-time kernels, RTOS (real-time operating system), Critical sections, Task management, Preemptive scheduling, Context switching, Interrupt management, Non-kernel-aware interrupt service routine (ISR), Processors with multiple interrupt priorities, The clock tick (or system tick), Wait lists, Time management, Resource management, Synchronization, Message passing, Flow control, Clients and servers, Memory management

UNIT - V — Lecture Hrs:

Software Reuse and Performance Engineering in Embedded Systems
Kinds of software reuse, Implementing reuse by layers,Arbitrary extensibility, Ebedded Software for Performance, The code optimization process, Using the development tools, Compiler optimization

Textbooks:

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COURSE STRUCTURE & SYLLABI

1. Software Engineering for Embedded Systems: Methods, Practical Techniques, and Applications, by Oshana, Robert; Kraeling, Mark, "Newnes" Publishers, 2013.
2. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", 3rd Edition, McGraw Hill Education, 2017

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COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED REAL TIME OPERATING SYSTEMS	L	T	P	C
21D06203c	Program Elective – III	3	0	0	3
	Semester	II			

Course Objectives:

- To provide broad understanding of the requirements of Real Time Operating Systems.
- To make the student understand, applications of these Real Time features using case studies.
- To use the real time operating system concepts.

Course Outcomes (CO): Student will be able to

- Acquire knowledge on Real Time features of UNIX and LINUX.
- Understand the basic building blocks of Real Time Operating Systems in terms of scheduling, context switching and ISR.
- Understand on Real Time applications using Real Time Linux, ucos2, VX works, Embedded Linux.

UNIT - I — Lecture Hrs:

Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II — Lecture Hrs:

Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

UNIT - III — Lecture Hrs:

Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT - IV — Lecture Hrs:

Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V — Lecture Hrs:

Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

Textbooks:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

Reference Books:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal,TMH, 2007.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

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COURSE STRUCTURE & SYLLABI

Course Code	HARDWARE AND SOFTWARE CO-DESIGN	L	T	P	C
21D06204a	Program Elective – IV	3	0	0	3
	Semester	II			

Course Objectives:

- To acquire the knowledge on various models of Co-design.
- To explore the interrelationship between Hardware and software in a embedded system
- To acquire the knowledge of firmware development process and tools during Co-design.
- To understand validation methods and adaptability.

Course Outcomes (CO): Student will be able to

- Acquire the knowledge on various models of Co-design.
- Explore the interrelationship between Hardware and software in a embedded system
- Acquire the knowledge of firmware development process and tools during Co-design.
- Understand validation methods and adaptability.

UNIT - I	Lecture Hrs:

Co- Design Issues
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II	Lecture Hrs:

Prototyping and Emulation
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III	Lecture Hrs:

Compilation Techniques and Tools for Embedded Processor Architectures
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV	Lecture Hrs:

Design Specification and Verification
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V	Lecture Hrs:

Languages for System – Level Specification and Design-I
System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Textbooks:

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COURSE STRUCTURE & SYLLABI

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009. 2. Hardware / Software Co- Design - Giovanni De Micheli, MariagiovannaSami,Kluwer Academic Publishers, 2002.
Reference Books:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010.

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COURSE STRUCTURE & SYLLABI

Course Code	ADHOC AND WIRELESS SENSOR NETWORKS	L	T	P	C
21D06204b	Program Elective – IV	3	0	0	3
	Semester	III			

Course Objectives:

- To understand the various wireless networks
- To analyze MAC, routing and transport layer protocols
- To learn about the concepts of wireless sensor networks

Course Outcomes (CO):

Students will be able to

- Understand the various wireless networks
- Analyze MAC, routing and transport layer protocols
- Learn about the concepts of wireless sensor networks

UNIT - I		Lecture Hrs:

Wireless LANs and PANs: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.
AD HOC WIRELESS NETWORKS: Introduction, Issues in Ad Hoc Wireless Networks

UNIT - II		Lecture Hrs:

MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT - III		Lecture Hrs:

Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT - IV		Lecture Hrs:

Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other TransportLayer Protocol for Ad Hoc Wireless Networks.

UNIT - V		Lecture Hrs:

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

Textbooks:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B. S. Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control – JagannathanSarangapani, CRC Press.

Reference Books:

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C. K. Toh, 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

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M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

Course Code	ALGORITHMS FOR VLSI DESIGN	L	T	P	C
21D06204c	Program Elective – IV	3	0	0	3
	Semester	II			

Course Objectives:

- To understand the VLSI design methodologies
- To understand the optimization methods
- To learn various methodologies in floor planning
- To explore the tools used in Physical Design Automation

Course Outcomes (CO):

- Understand the VLSI design methodologies
- Understand the optimization methods
- Learn various methodologies in floor planning
- Explore the tools used in Physical Design Automation

UNIT - I		Lecture Hrs:

PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT - II		Lecture Hrs:

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT - III		Lecture Hrs:

LAYOUT COMPACTION, PLACEMENT, FLOOR PLANNING AND ROUTING
Problems, Concepts and Algorithms.
MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT - IV		Lecture Hrs:

LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT - V		Lecture Hrs:

PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.
PHYSICAL DESIGN AUTOMATION OF MCMs
MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

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Textbooks:
1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY Student Edition, John wiley& Sons (Asia) Pvt. Ltd.1999. 2.Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed.,Springer International Edition, 2005.
Reference Books:
1. Computer Aided Logical Design with Emphasis on VLSI – Hill &Peterson,Wiley, 1993. 2.Modern VLSI Design :Systems on silicon – Wayne Wolf, 2nd Ed., Pearson Education Asia, 1998.

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COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEM DESIGN LAB	L	T	P	C
21D06205		0	0	4	2
	Semester	**II**			

Course Objectives:

- To familiarize with embedded systems programming concepts
- To implement different embedded communication and interfacing protocols

Course Outcomes (CO):

- Familiarize with embedded systems programming concepts
- Implement different embedded communication and interfacing protocols

List of Experiments:

1. Functional Testing of Devices
Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. Exporting Display on to other Systems
Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. GPIO Programming
Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. Interfacing Chronos eZ430
Chronos device is a programmable Texas Instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. ON/OFF Control Based On Light Intensity
Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. Battery Voltage Range Indicator
Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 LEDs, turn on 3 LED s for 2-3V, 2 LEDs for 1-2V, 1 LED for 0.1-1V & turn off all for 0V)
7. Dice Game Simulation
Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. Displaying RSS News Feed On Display Interface
Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. Porting Open w.r.t the Device
Attempt to use the device while connecting to a WiFi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. Hosting a website on Board
Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.

11. Webcam Server

Interfacing the regular USB webcam with the device and turn it into fully functional IP webcam & test the functionality.

12. FM Transmission

Transforming the device into a regular FM transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Software Requirements:

Keil / Python

Hardware Requirements:

Arduino/Raspbery Pi/Beaglebone

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COURSE STRUCTURE & SYLLABI

Course Code	VLSI SIMULATION LAB	L	T	P	C
21D06206		0	0	4	2
	Semester	II			

Course Objectives:

- To understand the design flow in VLSI
- To design and simulate a circuit for given specifications

Course Outcomes (CO):

- Understand the design flow in VLSI
- Design and simulate a circuit for given specifications

List of Experiments:

1. Dynamic Characteristics of CMOS Inverter
2. Design and Simulation of Combinational Circuits
   a) Generic Multiplexer.
   b) Generic Priority Encoder.
   c) Code Converters.
   d) Ripple Carry Adder.
   e) Carry-Look ahead adder.
   f) N-bit Comparator.
3. Design and Simulation of Sequential Circuits
   a) Shift Register with Load.
   b) Switch Debouncer.
   c) Timer.
   d) Fibonacci Series Generator.
   e) Frequency Meters.
4. Design and Simulation of Source Follower Circuits
5. Design and Simulation of Cascode Amplifier
6. Design and Simulation of Current Mirror Amplifier
7. Design and Simulation of Differential Amplifier

Software Requirements:
Micro Wind / Cadence / Electric / Mentor Graphics

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COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEMS PROTOCOLS	L	T	P	C
21D06301a	Program Elective – V	3	0	0	3
	Semester	III			

Course Objectives:

- To acquire knowledge on communication protocols of connecting Embedded Systems.
- To understand the design parameters of USB and CAN bus protocols.
- To understand the design issues of Ethernet in Embedded networks.
- To acquire the knowledge of wireless protocols in Embedded domain.

Course Outcomes (CO): Student will be able to

- Acquire knowledge on communication protocols of connecting Embedded Systems.
- Understand the design parameters of USB and CAN bus protocols.
- Understand the design issues of Ethernet in Embedded networks.
- Acquire the knowledge of wireless protocols in Embedded domain.

UNIT - I — Lecture Hrs:

Embedded Communication Protocols
Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT - II — Lecture Hrs:

USB and CAN Bus
USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT - III — Lecture Hrs:

Ethernet Basics
Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT - IV — Lecture Hrs:

Embedded Ethernet
Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT - V — Lecture Hrs:

Wireless Embedded Networking
Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

Textbooks:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference Books:

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COURSE STRUCTURE & SYLLABI

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - BhaskarKrishnamachari□, Cambridge press 2005.

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COURSE STRUCTURE & SYLLABI

Course Code	SOFT COMPUTING TECHNIQUES	L	T	P	C
21D06301b	Program Elective – V	3	0	0	3
	Semester	III			

Course Objectives:

- To understand the concepts of different types neural networks
- To understand the concepts of fuzzy logic systems
- To learn concepts of genetic algorithm

Course Outcomes (CO): Student will be able to

- Understand the concepts of different types neural networks
- Understand the concepts of fuzzy logic systems
- Learn concepts of genetic algorithm

UNIT - I		Lecture Hrs:

Fundamentals of Neural Networks & Feed Forward Networks: Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures.
Feed Forward Neural Network: Single Layer Feed Forward Neural Network, The Perceptron Model,
Multilayer Feed Forward Neural Network, Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT - II		Lecture Hrs:

Associative Memories & ART Neural Networks: Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture

UNIT - III		Lecture Hrs:

Fuzzy Logic & Systems: Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT - IV		Lecture Hrs:

Genetic Algorithms: Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT - V		Lecture Hrs:

Hybrid Systems: Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

Textbooks:

1.Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2.Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications -S.Rajasekaran, G.A. VijayalakshmiPai, July 2011, PHI, New Delhi.

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COURSE STRUCTURE & SYLLABI

3.Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006. 4.Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.
Reference Books:
1.Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi. 2.An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998 3.Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

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COURSE STRUCTURE & SYLLABI

Course Code	COMMUNICATION BUSES AND INTERFACES	L	T	P	C
21D06301c	Program Elective – V	3	0	0	3
	Semester	III			

Course Objectives:

- To understand the concepts of different types of serial buses.
- To learn about CAN, PCIe and USB architecture
- To learn about data streaming using serial communication protocols

Course Outcomes (CO): Student will be able to

- Understand the concepts of different types of serial buses.
- Learn about CAN, PCIe and USB architecture
- Learn about data streaming using serial communication protocols

UNIT - I		Lecture Hrs:

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features, Limitations and applications of RS232, RS485, I2C , SPI

UNIT - II		Lecture Hrs:

CAN ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT - III		Lecture Hrs:

PCIe
Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT - IV		Lecture Hrs:

USB
Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT - V		Lecture Hrs:

Data streaming Serial Communication Protocal- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

Textbooks:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2.Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

Reference Books:

1. USB Complete – Jan Axelson, Penram Publications.
2.PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

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COURSE STRUCTURE & SYLLABI

AUDIT COURSE-I

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COURSE STRUCTURE & SYLLABI

Course Code	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
21DAC101a		2	0	0	0
	Semester	I			

Course Objectives: This course will enable students:

- Understand the essentials of writing skills and their level of readability
- Learn about what to write in each section
- Ensure qualitative presentation with linguistic accuracy

Course Outcomes (CO): Student will be able to

- Understand the significance of writing skills and the level of readability
- Analyze and write title, abstract, different sections in research paper
- Develop the skills needed while writing a research paper

UNIT - I		Lecture Hrs:10

1Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity

UNIT - II		Lecture Hrs:10

Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization

UNIT - III		Lecture Hrs:10

Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

UNIT - IV		Lecture Hrs:9

Key skills needed for writing a Title, Abstract, and Introduction

UNIT - V		Lecture Hrs:9

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions

Suggested Reading

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

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COURSE STRUCTURE & SYLLABI

Course Code	DISASTER MANAGEMENT	L	T	P	C
21DAC101b		2	0	0	0
	Semester	I			

Course Objectives: This course will enable students:

- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluatedisasterriskreduction and humanitarian response policy and practice from Multiple perspectives.
- Developanunderstandingofstandardsofhumanitarianresponseandpracticalrelevanceinspecific types of disasters and conflict situations
- Criticallyunderstandthestrengthsandweaknessesofdisastermanagementapproaches,planningand programming in different countries, particularly their home country or the countries they work in

UNIT - I

Introduction:
Disaster:Definition,FactorsandSignificance;DifferenceBetweenHazardandDisaster;Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

UNIT - II

Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes,Volcanisms,Cyclones,Tsunamis,Floods,DroughtsandFamines,Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT - III

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering ADisasteror Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT - IV

Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. TechniquesofRiskAssessment,GlobalCo-OperationinRiskAssessmentand Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT - V

Disaster Mitigation:
Meaning,ConceptandStrategiesofDisasterMitigation,EmergingTrendsInMitigation.Structural Mitigationand Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Reading

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COURSE STRUCTURE & SYLLABI

1. R.Nishith,SinghAK,"DisasterManagementinIndia:Perspectives,issuesandstrategies
2. "'New Royal book Company..Sahni,PardeepEt.Al.(Eds.),"DisasterMitigationExperiencesAndReflections",PrenticeHall OfIndia, New Delhi.
3. GoelS.L.,DisasterAdministrationAndManagementTextAndCaseStudies",Deep&Deep Publication Pvt. Ltd., New Delhi

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COURSE STRUCTURE & SYLLABI

Course Code	SANSKRITFOR TECHNICAL KNOWLEDGE	L	T	P	C
21DAC101c		2	0	0	0
	Semester	**I**			

Course Objectives: This course will enable students:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- LearningofSanskrittodevelopthelogicinmathematics,science&othersubjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge
- Knowledge from ancientliterature

Course Outcomes (CO): Student will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science &technology can be understood
- Being a logical language will help to develop logic in students

UNIT - I

Alphabets in Sanskrit,

UNIT - II

Past/Present/Future Tense, Simple Sentences

UNIT - III

Order, Introduction of roots

UNIT - IV

Technical information about Sanskrit Literature

UNIT - V

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Suggested Reading

1.“Abhyaspustakam” –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi
2.“Teach Yourself Sanskrit” Prathama Deeksha- VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication
3.“India’s Glorious ScientificTradition” Suresh Soni, Ocean books (P) Ltd.,New Delhi

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M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS

COURSE STRUCTURE & SYLLABI

AUDIT COURSE-II

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COURSE STRUCTURE & SYLLABI

Course Code	PEDAGOGY STUDIES	L	T	P	C
21DAC201a		2	0	0	0
	Semester	**II**			

Course Objectives: This course will enable students:

- Reviewexistingevidenceonthereviewtopictoinformprogrammedesignandpolicy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes (CO): Student will be able to

Students will be able to understand:

- Whatpedagogicalpracticesarebeingusedbyteachersinformalandinformalclassrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumand guidance materials best support effective pedagogy?

UNIT - I

Introduction and Methodology: Aims and rationale, Policy back ground, Conceptual frame work and terminology Theories oflearning,Curriculum,Teachereducation.Conceptualframework,Research questions**.** Overview of methodology and Searching.

UNIT - II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT - III

Evidence on theeffectivenessofpedagogicalpractices,Methodologyfortheindepthstage:quality assessmen t of included studies. How can teacher education (curriculumandpracticum) andthescho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of th body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT - IV

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacherandthecommunity.Curriculumandassessment,Barrierstolearning:limitedresourcesand large class sizes

UNIT - V

Researchgapsandfuturedirections: Researchdesign**,**Contexts**,**Pedagogy**,**Teachereducation**,** Curriculum and assessment**,** Dissemination and research impact.

Suggested Reading

1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare, 31 (2): 245-261.
2. AgrawalM(2004)Curricularreforminschools:Theimportanceofevaluation,Journalof

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COURSE STRUCTURE & SYLLABI

3. Curriculum Studies, 36 (3): 361-379.
4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teachereducation research project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013)Improving teaching and learning of basic maths and reading in Africa: Does teacherpreparation count?International Journal Educational Development, 33 (3): 272–282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
   Chavan M (2003)ReadIndia: A mass scale, rapid, 'learning to read'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

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COURSE STRUCTURE & SYLLABI

Course Code	**STRESSMANAGEMENT BY YOGA**	**L**	**T**	**P**	**C**
21DAC201b		**2**	**0**	**0**	**0**
	Semester	**II**			

Course Objectives: This course will enable students:

- To achieve overall health of body and mind
- To overcome stres

Course Outcomes (CO): Student will be able to

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT - I		
Definitions of Eight parts of yog.(Ashtanga)		
UNIT - II		
Yam and Niyam.		
UNIT - III		
Do`sand Don't'sin life. i) Ahinsa,satya,astheya,bramhacharyaand aparigrahaii) Shaucha,santosh,tapa,swadhyay,ishwarpranidhan		
UNIT - IV		
Asan and Pranayam		
UNIT - V		
i)Variousyogposesand theirbenefitsformind &body ii)Regularizationofbreathingtechniques and its effects-Types ofpranayam		

Suggested Reading

1.'Yogic Asanas forGroupTarining-Part-I": Janardan SwamiYogabhyasiMandal, Nagpur
2."Rajayogaor conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

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COURSE STRUCTURE & SYLLABI

Course Code	PERSONALITY DEVELOPMENT THROUGHLIFE ENLIGHTENMENTSKILLS	L	T	P	C
21DAC201c		2	0	0	0
	Semester	**II**			

Course Objectives: This course will enable students:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes (CO): Student will be able to

- StudyofShrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityand achieve the highest goal in life
- The person who has studied Geetawilllead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT - I

Neetisatakam- Holistic development of personality
Verses-19,20,21,22(wisdom)
Verses-29,31,32(pride &heroism)
Verses-26,28,63,65(virtue)

UNIT - II

Neetisatakam- Holistic development of personality
Verses-52,53,59(dont's)
Verses-71,73,75,78(do's)

UNIT - III

Approach to day to day work and duties.
ShrimadBhagwadGeeta:Chapter2-Verses41,47,48,
Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,
Chapter18-Verses45,46,48.

UNIT - IV

Statements of basic knowledge.
ShrimadBhagwadGeeta:Chapter2-Verses 56,62,68
Chapter12 -Verses13,14,15,16,17,18
Personality of Rolemodel. Shrimad Bhagwad Geeta:

UNIT - V

Chapter2-Verses 17,Chapter3-Verses36,37,42,
Chapter4-Verses18,38,39
Chapter18– Verses37,38,63

Suggested Reading

1."SrimadBhagavadGita"bySwamiSwarupanandaAdvaitaAshram(PublicationDepartment), Kolkata
2.Bhartrihari'sThree Satakam (Niti-sringar-vairagya) by P.Gopinath, RashtriyaSanskrit Sansthanam, New Delhi.

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COURSE STRUCTURE & SYLLABI

OPEN ELECTIVE

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COURSE STRUCTURE & SYLLABI

Course Code	INDUSTRIAL SAFETY	L	T	P	C
21DOE301b		3	0	0	3
Semester		III			

Course Objectives:

- To know about Industrial safety programs and toxicology, Industrial laws , regulations and source models
- To understand about fire and explosion, preventive methods, relief and its sizing methods
- To analyse industrial hazards and its risk assessment.

Course Outcomes (CO): Student will be able to

- To list out important legislations related to health, Safety and Environment.
- To list out requirements mentioned in factories act for the prevention of accidents.
- To understand the health and welfare provisions given in factories act.

UNIT - I — Lecture Hrs:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT - II — Lecture Hrs:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT - III — Lecture Hrs:

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working andapplications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT - IV — Lecture Hrs:

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V — Lecture Hrs:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Textbooks:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

Reference Books:

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

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COURSE STRUCTURE & SYLLABI

Course Code	BUSINESS ANALYTICS	L	T	P	C
21DOE301c		3	0	0	3
	Semester	**III**			

Course Objectives:

- The main objective of this course is to give the student a comprehensive understanding of business analytics methods.

Course Outcomes (CO): Student will be able to

- Students will demonstrate knowledge of data analytics.
- Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
- Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

UNIT - I — Lecture Hrs:

Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst.
Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts.

UNIT - II — Lecture Hrs:

Life Cycles: Systems Development Life Cycles, Project Life Cycles, Product Life Cycles, Requirement Life Cycles.

UNIT - III — Lecture Hrs:

Forming Requirements: Overview of Requirements, Attributes of Good Requirements, Types of Requirements, Requirement Sources, Gathering Requirements from Stakeholders, Common Requirements Documents.Transforming Requirements: Stakeholder Needs Analysis, Decomposition Analysis, Additive/Subtractive Analysis, Gap Analysis, Notations (UML & BPMN), Flowcharts, Swim Lane Flowcharts, Entity-Relationship Diagrams, State-Transition Diagrams, Data Flow Diagrams, Use Case Modeling, Business Process Modeling

UNIT - IV — Lecture Hrs:

Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements. Managing Requirements Assets: Change Control, Requirements Tools

UNIT - V — Lecture Hrs:

Recent Trands in: Embedded and colleborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism.

Textbooks:

1. Business Analysis by James Cadle et al.
2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray

Reference Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

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COURSE STRUCTURE & SYLLABI

Course Code	WASTE TO ENERGY	L	T	P	C
21DOE301e		3	0	0	3
	Semester	III			

Course Objectives:

- Introduce and explain energy from waste, classification and devices to convert waste to energy.
- To impart knowledge on biomass pyrolysis, gasification, combustion and conversion process.
- To educate on biogas properties ,bio energy system, biomass resources and their classification and biomass energy programme in India.

Course Outcomes (CO): Student will be able to

- To know about overview of Energy to waste and classification of waste.
- To acquire knowledge on bio mass pyrolysis, gasification, combustion and conversion process in detail.
- To gain knowledge on properties of biogas, biomass resources and programmes to convert waste to energy in India.

UNIT - I — Lecture Hrs:10

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT - II — Lecture Hrs:10

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT - III — Lecture Hrs:12

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation

UNIT - IV — Lecture Hrs:12

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT - V — Lecture Hrs:10

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification -
Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Textbooks:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., TMH, 2017

Reference Books:

1. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley

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& Sons, 1996
Online Learning Resources:
https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/ https://www.youtube.com/watch?v=x2KmjbCvKTk