JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

COURSE STRUCTURE AND SYLLABUS

(For Affiliated Engineering Colleges w.e.f. 2017-18 Admitted Batch)

M.TECH-ECE-VLSI & EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI, VLSI & EMBEDDED SYSTEM DESIGN (VLSI&ES, ES&VLSI, VLSI&ESD)

M.Tech I Semester

S.No	Subject Code	Subject	L	T	P	C
1.	17D06101	Structural Digital System Design	4	-	-	4
2.	17D06201	Embedded System Design	4	-	-	4
3.	17D68101	CMOS Analog and Digital IC Design	4	-	-	4
4.	17D55101	Embedded C	4	-		4
5.	17D57104 17D06103 17D57105	**Elective-I** a. VLSI Signal Processing b. Advanced Computer Architecture c. CAD for VLSI	3	-	-	3
6.	17D06202 17D38201 17D06208	**Elective-II** a. CPLD and FPGA Architectures and Applications b. Wireless Communications and Networks c. Network Security and Cryptography	3	-	-	3
7.	17D38107	Structural Digital System Design Lab	-	-	3	2
8.	17D38202	Embedded System Design Lab	-	-	3	2
		TOTAL	**22**	**-**	**06**	**26**

M.Tech II Semester

S.No	Subject Code	Subject	L	T	P	C
1.	17D57201	Low Power VLSI Design	4	-	-	4
2.	17D57202	CMOS Mixed Signal Design	4	-	-	4
3.	17D55203	ARM Based Embedded system Design	4	-	-	4
4.	17D55202	Embedded Networking	4	-		4
5.	17D55201 17D06209 17D06205	**Elective-III** a. System on Chip Architecture b. Digital Image and Video Processing c. Internet Protocols	3	-	-	3
6.	17D55206 17D06206 17D55204	**Elective-IV** a. ASIC Design b. MEMS and its Applications c. Hardware Software Co-Design of Embedded System	3	-	-	3
7.	17D57207	VLSI System Design Lab	-	-	3	2
8.	17D55207	ARM Based Embedded System Design Lab	-	-	3	2
		TOTAL	**22**	**-**	**06**	**26**

M.Tech. II YEAR (III Semester)

S. No	Course Code	Subject	L	T	P	C
1.	 17D20301 17D20302 17D20303	Elective – V (Open Elective) 1. Research Methodology 2. Human Values & Professional Ethics 3. Intellectual Property Rights	4	---	---	4
2.	17D68301	ELECTIVE – VI (MOOCs)	--	---	---	--
3.	17D68302	Comprehensive Viva Voce	--	---	---	2
4.	17D68303	Seminar	--	---	---	2
5.	17D68304	Teaching Assignment	--	---	---	2
6.	17D68305	Project Work Phase I	--	---	---	4
	Total		4			14

M.Tech. II YEAR (IV Semester)

S. No	**Course Code**	**Subject**	**L**	**T**	**P**	**C**
1.	17D68401	Project Work Phase II	--	---	---	12
	Total					**12**

Project Viva Voce Grades:

A: Satisfactory

B: Not Satisfactory

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year I Semester (VLSI &ES)

L	T	P	C
4	0	0	4

(17D06101) STRUCTURED DIGITAL SYSTEM DESIGN

Course Objective:

- To study about structural functionality of different Digital blocks (Both combinational and Sequential)
- To provide an exposure to ASM charts, their notations and their realizations.
- To provide an exposure to VHDL and different styles of modeling using VHDL.
- To introduce the concept of micro programming and study issues related to micro programming

Course Outcome:

After Completion of this course, students will be able to

- Understand structural functionality of different digital blocks
- Represent and Realize their designs in ASM charts
- Represent their designs in different modeling styles by using VHDL
- Understand concept of Micro program and issues related to micro programming

UNIT-1

BUILDING BLOCKS FOR DIGITAL DESIGN: Multiplexer, De-multiplexer, Decoder, Encoder, Comparator, Adder, ALU, Carry-look-ahead adder.

BUILDING BLOCKS WITH MEMORY: Clocked building blocks, register building blocks, RAM, ROM, PLA, PAL, Timing devices.

UNIT -II

DESIGN METHODS: Elements of design style, top-down design, separation of controller and architecture, refining architecture, and control algorithm, Algorithmic State Machines, ASM chart notations.

UNIT-III

REALISING ASMS - Traditional synthesis from ASM chart, multiplexer controller method, one-shot method, ROM based method.

ASYNCHRONOUS INPUTS AND RACES - Asynchronous ASMs, Design for testability, test vectors, fault analysis tools.

UNIT-IV

MICROPROGRAMED DESIGN: Classical Microprogramming with Modem Technology; Enhancing the Control Unit; The 2910 Microprogram Sequencer; Choosing a Microprogram Memory; A Development System for Microprogramming; Designing a Microprogrammed Minicomputer

UNIT-V

MODELLING WITH VHDL: CAD tools, simulators, schematic entry, synthesis from VHDL.

DESIGN CASE STUDIES: Single pulse, system clock, serial to parallel data conversion, traffic light controller.

TEXT BOOKS:

1. Franklin P. Prosser and David E. Winkel, "The Art of Digital Design", Prentice Hall.
2. Roth, “Digital System Design using VHDL”, Mc. Graw Hill, 2000

REFERENCE BOOKS:

1. William Fletcher, An Engineering Approach to Digital Design, 1st Edition, Prentice-Hall India, 1997.
2. William J Dally and John W Poulton, Digital Systems Engineering, Cambridge University Press, 2008.
3. Jayaram Bhasker, A VHDL Primer, 3rd edition, Prentice-Hall India, 2009.
4. VHDL for Programmable Logic - Kevin Skahill, Cypress Semiconductors

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D06201) EMBEDDED SYSTEM DESIGN

Course Outcomes:

After completion of this course the students will be able to understand

- The issues relating to hardware and software design concepts associated with processor in Embedded Systems.
- The concept of low power microcontrollers.
- The hardware software co- design issues pertaining to design of an Embedded System using low power microcontrollers.

UNIT – I

Introduction to Embedded Electronic Systems and Microcontrollers:

An Embedded System-Definition, Embedded System Design and Development Life Cycle, An Introduction to Embedded system Architecture, The Embedded Systems Model, Embedded Hardware, The Embedded Board and the von Neumann Model, Embedded Processors: ISA Architecture Models, Internal Processor Design, Processor Performance, Board Memory: Read-Only Memory (ROM), Random-Access Memory (RAM), Auxiliary Memory, Memory Management of External Memory and Performance, Approaches to Embedded Systems, Small Microcontrollers, Anatomy of a Typical Small Microcontroller, Small Microcontrollers Memory, Embedded Software, Introduction to small microcontroller (MSP430).

UNIT-II

MSP430 – I:

Architecture of the MSP430 Processor: Central Processing Unit, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Examples, Reflections on the CPU and Instruction Set, Resets, Clock System, Memory and Memory Organization.

Functions, Interrupts, and Low-Power Mode: Functions and Subroutines, Storage for Local Variables, Passing Parameters to a Subroutine and Returning a Result, Mixing C and Assembly Language, Interrupts, Interrupt Service Routines, Issues Associated with Interrupts, Low-Power Modes of Operation.

UNIT – III

MSP430 – II:

Digital Input, Output, and Displays: Parallel Ports, Digital Inputs, Switch Debounce, Digital Outputs, Interface between Systems, Driving Heavier Loads, Liquid Crystal Displays, Simple Applications of the LCD.

Timers: Watchdog Timer, Timer_A, Timer_A Modes, Timer_B,Timer_B Modes, Setting the Real-Time Clock, State Machines.

UNIT – IV

MSP430 Communication:

Communication Peripherals in the MSP430, Serial Peripheral Interface, SPI with the USI, SPI with the USCI, AThermometer Using SPI Modes,Inter-integrated Circuit Bus(I^2C) and its operations, State Machines for I^2C Communication, AThermometer Using I^2C, Asynchronous Serial Communication, Asynchronous Communication with the USCI_A, ASoftware UART Using Timer_A, Other Types of Communication.

UNIT – V

MSP430 Case Studies:

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I2C.

TEXT BOOKS:

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.

2. John H. Davies "MSP430 Microcontroller Basics",Elsevier Ltd Publications, Copyright 2008.

REFERENCE BOOKS

1. Manuel Jiménez Rogelio,PalomeraIsidoroCouvertier "Introduction to Embedded SystemsUsing Microcontrollers and the MSP430" Springer Publications, 2014.

2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.

3. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.

4. Arnold S Burger, "Embedded System Design", CMP Books, 2002.

5. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications,Second Edition, 2008.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D68101) CMOS ANALOG AND DIGITAL IC DESIGN

Course Outcomes:

After completion of the course the students will be able to

- Understand significance of different biasing styles and apply them for designing analog ICs.
- Analyze the functionality of Current Mirrors, Current Sinks, Differential amplifiers and Current amplifiers.
- Design basic building blocks of analog ICs like, current mirrors, current sources, current sinks, two stage CMOS Power amplifiers and comparators.
- Realize and implement basic combinational and sequential elements that are commonly observed in digital ICs.
- Design basic combinational and sequential elements using NMOS and CMOS design strategies.
- Analyze the dynamic performance of CMOS circuits

UNIT –I

MOS Device Modeling: CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Sub-threshold MOS Model.

Analog CMOS Sub-Circuits: Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage REFERENCE BOOKS, Band gap Reference.

UNIT-II

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Alternative definition of CMRR.

UNIT –III

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT –IV

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, CMOS transmission gates, Designing with Transmission gates.

UNIT –V

Sequential MOS Logic Circuits: Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
4. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce,
3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.
4. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRCPress, 2011
5. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan,BorivojeNikolic, 2nd Ed., PHI.

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D55101) EMBEDDED C

Course Outcomes

After completion of the course students able to

- Know about programming concepts in embedded system design
- Understand features and concepts of embedded programming languages and
- Able describe how microcontroller based embedded systems are programmed and implemented in real time applications.
- Write simple programs and implement the same embedded hardware.

UNIT – I

Programming Embedded Systems in C Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions Introducing the 8051 Microcontroller Family Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT – II

Reading Switches Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III

Adding Structure to the Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV

Meeting Real-Time Constraints Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V

Compilation and linking, Compiling and Linking Multiple Source Files, Compiling Multifile Programs, Linking Multifile Programs, Using #include, External VariablesUsing an Object Library Manager Using MAKE Files.

Case Study: Intruder Alarm System Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008

2. Advanced C - Peter D. Hipson, Sams Publishing, USA, 1992

REFERENCE BOOKS

1. PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D57104) VLSI SIGNAL PROCESSING
Elective-I

Course Outcomes:

After completion of the course the students will be able to

- Get in depth knowledge on signal processing system and various techniques of power reduction.
- Realize various adders, multipliers and filters and optimize their operation of by reducing the redundant operations
- Apply concept of pipelined architecture for various combinational and sequential circuit modules like adders, multipliers, filters
- Design Low Power IIR filters

UNIT-I

Transformations for retiming.Folding and unfolding DSP programs.

UNIT-II

Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters. Bit serial multipliers. Bit serial filter design and implementation . Canonic signed digit arithmetic, Distributed arithmetic.

UNIT-III

Redundant arithmetic, redundant number representations , carry free radix 2 addition and subtraction . Hybrid radix 4 addition. Radix 2 hybrid redundant multiplication architectures , data format conversion. Redundant to nonredundant converter.Numerical strength reduction.

UNIT-IV

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems.Asynchronous pipelining.

UNIT-V

Scaling versus power consumption. Power analysis, power reduction techniques, power estimation techniques. Low power IIR filter design .Low power CMOS lattice IIR filter.

TEXT BOOKS:

1. K.K. Parhi : VLSI Digital Signal Processing systems, John Wiley, 1999.

2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D06103) ADVANCED COMPUTER ARCHITECTURE
Elective-I

Course Outcomes:

After completion of the course the students will be able to

- Know about different parallel computer models and their network properties.
- Understand about different concepts related to pipelining and super scalar techniques.
- Get complete knowledge regarding multi processors and multi computers.

UNIT - I

Parallel Computer Models – System attributes to performance, Multiprocessors and Multicomputers, Classifications of Architectures, Multivector and SIMD Computers, Architecture development tracks

UNIT - II

Program and Network Properties- Conditions for parallelism, Program partitioning and Scheduling, Program flow mechanisms, System interconnect architectures, Performance metrics and measures, Parallel Processing Applications

UNIT-III

Processors and Memory Hierarchy- Advanced Processor Technology, Superscalar and Vector processors, Memory hierarchy technology, Virtual Memory, Backplane bus systems, Cache memory organizations, Shared memory organizations

UNIT - IV

Pipelining and Superscalar Techniques Linear Pipeline processors, Nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design, Superscalar and Super Pipeline Design

UNIT- V

Multiprocessors and Multicomputers Multiprocessor System Interconnects, Cache Coherence and Synchronization mechanisms, Three generations of Multicomputers, Message passing mechanisms, Vector Processing principles, Principles of Multithreading

TEXT BOOKS:

1. Hwang kai, "Advanced Computer Architecture", McGraw-Hill, 2001.
2. Patterson, David and Hennessy John**,** Morgn Kaufmann, "Computer Architecture",2001.

REFERENCE BOOKS:

1. William Stallings, Computer Organization and Architecture, 8th Edition, Prentice-Hall India, 2010.
2. David A Patterson and John L. Hennesey, Computer Organization and Design, 4th Edition, Elsevier India, 2011.
3. Andrew S Tanenbaum and James R Goodman, Structured Computer Organization, 5th Edition PrenticeHall India, 2009.

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D57105) CAD FOR VLSI
Elective-I

Course Outcomes:
After completion of the course the students will be able to

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- Practice the application of fundamentals of VLSI technologies
- Optimize the implemented design for area, timing and power by applying suitable constraints.
- Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on reconfigurable hardware platform (FPGA)
- Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.
- Develop various algorithms at various levels of physical design.

UNIT-I
VLSI Physical Design Automation : VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II
Partitioning, Floor Planning, Pin Assignment and Placement : Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.
Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments. Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

UNIT-III
Global Routing and Detailed Routing : Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-IV
Physical Design Automation of FPGAs and MCMs : FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT –V
Chip Input and Output Circuits : ESD Protection, Input Circuits, Output Circuits, Noise in Circuits, On Chip Clock Generation and Distribution, Latch – Up and its prevention.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by NaveedShervani, 3rd Edition, 2005, Springer International Edition.

2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.

2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.

3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D06202) CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
Elective-II

Course Outcomes:

After completion of the course students able to

- Understand the features and architectures of industrial CPLDs with different families.
- Understand the features and architectures of industrial FPGAs with different families.
- Know the programming techniques used in FPGA design methodology.
- Design and implement complex real time digital circuits.

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT –III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT –V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

REFERENCE BOOKS

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D38201) WIRELESS COMMUNICATIONS AND NETWORKS
Elective-II

Course Outcomes
After completion of the course students able to

- Understand concepts of wireless communication systems and their applications.
- Know about the mobile radio propagation techniques and detailed understanding in wireless mobile communication.
- Understand communication networks and detailed analysis of wireless communications networks.
- Understand the different protocols used for wireless communication systems and networks.

UNIT –I The Cellular Concept-System Design Fundamentals:
Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT –II Mobile Radio Propagation:
Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- LongleyRyce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT –III Mobile Radio Propagation:
Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT –IV Equalization and Diversity:
Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT –V Wireless Networks:

Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – GottapuSasibhushanaRao, Pearson Education, 2012.

REFERENCE BOOKS

1. Principles of Wireless Networks – KavehPahLaven and P. Krishna Murthy, 2002, PE
2. Wireless Digital Communications – KamiloFeher, 1999, PHI.
3. Wireless Communication and Networking – William Stallings, 2003, PHI.

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M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D06208) NETWORK SECURITY AND CRYPTOGRAPHY

Elective-II

Course Outcomes:

After completion of this course students will be able to know

- The need and role of security and cryptography in computer networks.
- Gain knowledge about different techniques associated with encryption.
- Functioning of different algorithms associated with computer networks.
- Gain knowledge regarding different security architecture and designing issues related to fire walls.

UNIT – I

Introduction: Attacks, services and mechanisms, security attacks, security services, a model for internet work security, protection through cryptography, the role of cryptography in network security.

UNIT – II

Conventional Encryption: Substitution techniques and transposition techniques, block cipher principles, block cipher design principles, block cipher modes of operation. The data encryption standard

UNIT – III

Public-key encryption: Principles of public-key cryptosystems, the RSA algorithm, key management. Authentication requirements, authentication functions, message authentication codes, hash functions.

UNIT – IV

Digital Signatures and Authentication Protocols: Digital signatures, Digital signature standard, Authentication Protocols, MD5, message digest algorithm, secure hash algorithm, HMAC.

UNIT – V

Mall security & IP security: Pretty good privacy, IP security overview, IP security architecture, Intruders, viruses and related threats, firewall design principles

TEXT BOOKS:

1. W. Stallings**, "**Cryptography & Network Security", 3/e, PHI, 2003
2. Eric Maiwald**, "**Fundamental of Network Security", Dreamtech press Osborne MGH, 2004

REFERENCE BOOKS:

1. Sean Convery, " Network Security Architectures, Published by Cisco Press, First Ed. 2004.
2. AtulKahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.
3. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
4. Stewart S. Miller, "Wi-Fi Security", McGraw Hill, 2003.
5. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security In Computing", 3rd Edition, Pearson Education, 2003.
6. Jeff Crume, "Inside Internet Security" Addison Wesley, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

(17D38107) STRUCTURAL DIGITAL SYSTEM DESIGN LAB

Course Objective:

- To understand about VHDL and Verilog Programming in all available styles.
- To understand differences between Verilog and VHDL.
- To represent the different digital blocks in verilog and VHDL in all available styles of modelling

Course Outcome:

After completion of this course the students will be able to understand

- Different modeling styles available in VHDL and Verilog and difference between them
- Difference between verilog and VHDL
- Representation of different digital modules in different modelling styles available in VHDL and Verilog

Using VHDL or Verilog do the following experiments

1. Design of 4-bit adder / subtractor
2. Design of Booth Multiplier
3. Design of 4-bit ALU
4. Design SISO, SIPO, PISO, PIPO Registers
5. Design of Ripple, Johnson and Ring counters
6. Design of MIPS processor
7. Design of Washing machine controller
8. Design of Traffic Light Controller
9. Design “1010” pattern detector using Mealy state Machine
10. Design “1100” recursive pattern detector using Moore state Machine
11. Design simple Security System Using FSM/ASM
12. Mini Project

Tools Required:

VHDL or VERILOG

Hardware Required:

Computers with latest Configuration.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year I Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

(17D38202) EMBEDDED SYSTEM DESIGN LAB

List of Experiments

PART – A

Using Embedded C

Note: Any 10 Programs form the following

1. Write a simple program to print "hello world"
2. Write a simple program to show a delay.
3. Write a loop application to copy values from P1 to P2
4. Write a c program for counting the no of times that a switch is pressed & released.
5. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.
6. Write a program to create a portable hardward delay.
7. Write a c program to test loop time outs.
8. Write a c program to test hardware based timeout loops.
9. Develop a simple EOS showing traffic light sequencing.
10. Write a program to display elapsed time over RS-232 link.
11. Write a program to drive SEOS using Timer 0.
12. Develop software for milk pasteurization system.

PART – B

Note. Any 6 Programs from the following (Experiment – 1 is mandatory)

1. A Study of Code Composer Studio (CC Studio Latest Version)
2. Flashing a light by a software delay.
3. Displaying Characters on LCD.
4. Serial Communication using UART.
5. Basic Input and Output using MSP430 UART.
6. Interrupt Handling using MSP430.
7. Analog to Digital Conversion using MSP430.
8. Interfacing external Devices to GPIO Ports

Equipment Required:

1. Computer with latest configurations
2. Code Composer Studio v6.1 (Preferably Latest version)
3. MSP430/ARM based Hardware kits and add-on boards.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D57201) LOW POWER VLSI DESIGN

Course Outcomes :

After completion of this subject, students will be able to

- Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- Implement Low power design approaches for system level and circuit level measures.
- Design low power adders, multipliers and memories for efficient design of systems.

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry LookAhead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, BaughWooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1.CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.

2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D57202) CMOS MIXED SIGNAL DESIGN

Course outcomes:

After the Completion of the course the students will be able to

- Demonstrate first order filter with least interference
- Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT-I

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-V

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibitquantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D55203) ARM BASED EMBEDDED SYSTEM DESIGN

Course Objective:

- To get knowledge in system design using Micro controllers
- To Study the architectural features and and programming aspects of ARM controllers/processors.
- To learn about memory management in the system design applications

Course Outcome:

After completion of this course students will be able to

- Gets complete knowledge about the system design concepts using Micro controllers.
- Understand thoroughly the architectural and programming concepts of ARM controllers.
- Know about the memory management concepts in system design

UNIT – I

ARM Embedded Systems:

An Embedded System-Definition, Embedded System Design and Development, Life Cycle, Embedded system Architecture, Embedded Systems classification, The RISC Design Philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software, ARM processor Families, Core extensions, Architecture Revisions.

UNIT-II: ARM Programming Model-I

Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-III: ARM Programming Model-II

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT-IV : ARM Programming

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT-V: Memory Management

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

TEXT BOOKS:

1. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM Systems Developer's Guide- Designing & Optimizing System Software", 2008, Elsevier.
2. Jonathan W. Valvano – Brookes / Cole, 1999, "Embedded Microcomputer Systems, Real Time Interfacing", Thomas Learning.

REFERENCE BOOKS:

1. Intel and ARM Data Books on Microcontrollers.
2. Embedded System Design-Frank Vahid/Tony Givargis, John Willey, 2005.
3. Microcontroller (Theory and Applications) Ajay V Deshmukh, Tata McGraw-Hill, 2005.
4. An Embedded Software Primer-David E.Simon, Pearson Education, 1999.

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
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(17D55202) EMBEDDED NETWORKING

Course Outcomes:

- Able to understand the basic working modes of networks and its formatted data frames, its control
- Able to understand the significance of embedded networks in real time applications and to use it for specific applications.
- Able to Know different types of communication protocols like serial and parallel communication protocols
- Able to know different types of communication protocols which have embedded end modules
- Able to understand wired and wireless communication protocols, its formats
- Able to understand and gain knowledge on wireless sensors and its application in wireless embedded networks

UNIT –I

Embedded Communication Protocols:

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II

USB and CAN Bus:

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III

Ethernet Basics:

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV

Embedded Ethernet:

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V

Wireless Embedded Networking:

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - BhaskarKrishnamachari, Cambridge press 2005.

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D55201) SYSTEM ON CHIP ARCHITECTURE

Elective-III

Course Outcomes:

After completion of this course the students will be able to

- Get complete basics related to SoC architecture and different approaches related to SoC Design.
- Able to select an appropriated robust processor for SoC Design
- Able to Select an appropriate memory for SoC Design.
- Design SoC
- Realize real time case studies

UNIT I:

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II:

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III:

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV:

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V:

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

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M.Tech I year II Semester (VLSI &ES) **L T P C**

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(17D06209) DIGITAL IMAGE AND VIDEO PROCESSING

Elective-III

Course Outcomes:

- Able to design pattern recognition systems.
- Design and implement feature extraction techniques for a given application.
- Design a suitable classifier for a given application.

UNIT-I

IMAGE FUNDAMENTALS AND TRANSFORMS

Image Representation- Sampling and Quantization - Two dimensional DFT- Discrete cosine Transform - Walsh - Hadamard transform - Wavelet transform - Construction of Wavelets-Types of wavelets - principal component analysis.

UNIT -II

PROCESSING AND MODELING OF IMAGES

Pre-processing -Point operations – contrast stretching – Histogram - Histogram equalization - Image segmentation- pixel based, edge based, region based segmentation - Morphological image processing - Edge and texture models - Image registration - Colour Image Processing –

UNIT-III

SPATIAL FEATURE EXTRACTION

Feature selection - Localized feature extraction- Boundary Descriptors - Moments - Texture Descriptors - Co-occurrence features

UNIT-IV

CLASSIFIERS

Kernel based approaches - clustering methods - Maximum Likelihood Estimation- Bayesian approach- Pattern Classification

UNIT-V

VIDEO OBJECT EXTRACTION

Back ground subtraction – Frame difference - Static and dynamic background modeling - optical flow techniques-Handling occlusion- scale and appearance changes - Shadow removal.

TEXT BOOKS:

1. A.K.Jain, “Fundamentals of Digital Image Processing”, Prentice-Hall, 2002.
2. R.C.Gonzalez and R.E.Woods, „Digital Image Processing‟, Second Edition, Pearson Education, 2002.
3. A.Bovik, “Handbook of Image and Video Processing”, 2nd Edition, Academic Press, 2005.

REFERENCE BOOKS:

1. Mark Nixon and Alberto Aguado, “Feature Extraction and Image Processing”, Academic Press, 2008.
2. John C.Russ, “The Image Processing Handbook”, CRC Press, 2007.
3. Richard O. Duda, Peter E. Hart and David G. Stork., “Pattern classification”, Wiley, 2001

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D06205) INTERNET PROTOCOLS
Elective-III

Course Outcomes:

- Gets familiar with the Internetworking concepts, internet addressing and TCP/IP protocol Suite.
- Understand Mobile IP and multicasting & unicasting routing protocols.
- Understand the IP security and the firewalls.

UNIT -I

Internetworking Concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of thee Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address: Classful Addressing: Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting

Classless Addressing: Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router.

ARP and RARP: ARP, ARP Package, RARP.

UNIT -II

Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.

Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.

Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

UNIT –III

Unicast Routing Protocols (RIP, OSPF, and BGP): Intra and Inter domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.

Multicasting and Multicast Routing Protocols: Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

UNIT -IV:

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.

Remote Login TELNET: Concept, Network Virtual Terminal (NVT).

File Transfer FTP and TFTP: File Transfer Protocol (FTP).

Electronic Mail: SMTP and POP.

Network Management-SNMP: Concept, Management Components, World Wide Web- HTTP Architecture.

UNIT –V

Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/ Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:

1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3 rd edition PHI

REFERENCE BOOKS:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.
5. The Internet and Its Protocols – AdrinFarrel, Elsevier, 2005.

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D55206) ASIC DESIGN
Elective-IV

Course Outcomes:

After completion of the course the student will be able to

- Understand different types of ASICs and their libraries.
- Understands about programmable Asics, I/O modules and their interconnects.
- Gets complete knowledge regarding different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT I

INTRODUCTION TO ASICs:

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT II

PROGRAMABLE ASICS AND PROGRAMABLE ASIC LOGIC CELLS:

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III

I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE:

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT IV

LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS:

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Senthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT V

SIMULATION, TEST AND ASIC CONSTRUCTION:

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

TEXT BOOKS:

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L.J.Herbst, “Integrated Circuit Engineering”, Oxford Science Publications, 1996.

REFERENCE BOOKS:

1. Himanshu Bhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design compiler”, 2nd Edition, Kluwer Academic, 2001.

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D06206) MEMS AND ITS APPLICATIONS
Elective-IV

Course Outcomes:

After completion of this course the students will be able to

- Understand concepts of basic MEM devices and systems
- Acquires knowledge on mechanical terms used in MEMS
- Understand the two terminal MEMS and its characteristics.
- Design digital and analog applications in various silicon based MEMS structures

UNIT - I

Introduction Basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT - II

Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, Distributed force, distributed force, Deflection curves for canti-levers- fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – Transient response of the MEMS.

UNIT-III

Types Two terminal MEMS - capacitance Vs voltage Curve – Variable capacitor. Applications of variable capacitors. Two terminal MEM structures. Three terminal MEM structures – Controlled variable capacitors – MEM as a switch and possible applications. UNIT-IV MEM Circuits & Structures MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR, simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS.

UNIT-V

MEM Technologies Silicon based MEMS- Process flow – Brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies. Metal Based MEMS: Thin and thick film technologies for MEMS. Process flow and description of the processes, Status of MEMS in the current electronics scenario.

TEXT BOOKS

1. MEMS Theory, Design and Technology - GABRIEL. M.Review, R.F.,2003, John wiley& Sons. .

2. Strength of Materials –ThimoShenko, 2000, CBS publishers & Distributors. 3. MEMS and NEMS, Systems Devices; and Structures - ServeyE.Lyshevski, 2002, CRC Press.

REFERENCE BOOKS

1. Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House, London.

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M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
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(17D55204) HARDWARE SOFTWARE CO-DESIGN OF EMBEDDED SYSTEM
Elective-IV

Course outcomes:
After completion of this course the students will be able to

- Analyze and apply design methodologies.
- Appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their interrelationships.
- Get familiar with modern hardware/software tools for building prototypes and to be able to demonstrate practical competence in these areas

UNIT I NATURE OF HARDWARE AND SOFTWARE
Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Transformations.

UNIT II DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE
Software Implementation of Data Flow – Converting queues and actors into software, Dynamic Scheduler – Hardware Implementation of Data Flow – single rate SDF graphs into hardware, Pipelining – Analysis of control flow and data flow – construction of control and data flow graph – Translating C into hardware – Designing data path and controller.

UNIT III DESIGN SPACE OF CUSTOM ARCHITECTURES
Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT IV HARDWARE/ SOFTWARE INTERFACES
Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer‟s model.

UNIT V CASE STUDIES TriviumCripto coprocessor – Trivium stream cipher algorithm, Trivium for 8-bit platforms – AES coprocessor, CORDIC coprocessor – algorithm and implementation.

TEXT BOOKS:

1. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf, ”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub, 1997.

REFERENCE BOOKS:

1. Giovanni De Micheli, Rolf Ernst Morgon, ”Reading in Hardware/Software Co-Design“ Kaufmann Publishers, 2001.
2. Patrick Schaumont, A Practical Introduction to Hardware/Software Codesign, 2nd Edition, Springer, 2010.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

(17D57207) VLSI SYSTEM DESIGN LAB

Learning Outcomes:

After completion of this course the students will be able to

- Understand syntax of various commands available with verilog and fundamental associated with design of digital systems
- To design and simulate and implement various digital system like traffic light controller, UART.
- Able develop problem solving skills and adapt them to solve real world problems
- Write scripts using perl for building digital blocks

The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM.
5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.
9. Fire Detection and Control System using Combinational Logic circuits.
10. Traffic Light Controller using Sequential Logic circuits
11. Pattern Detection using Moore Machine.
12. Finite State Machine (FSM) based logic circuit.
13. Perl Programming for basic operations.

Lab Requirements:

Software:

Xilinx ISE Suite, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Perl Software.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year II Semester (VLSI &ES)	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

(17D55207) ARM BASED EMBEDDED SYSTEM DESIGN LAB

The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.

- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.
- The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

List of Experiments:

Part-I

Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II

Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.

(ii) LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

(i) The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.

(ii) Serial Cables, Network Cables and recommended power supply for the board.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech III semester (VLSI &ES) **L T P C**

4 0 0 4

(17D20301) RESEARCH METHODOLOGY
(Elective V-OPEN ELECTIVE)

UNIT I

Meaning of Research – Objectives of Research – Types of Research – Research Approaches – Guidelines for Selecting and Defining a Research Problem – research Design – Concepts related to Research Design – Basic Principles of Experimental Design.

UNIT II

Sampling Design – steps in Sampling Design –Characteristics of a Good Sample Design – Random Sampling Design.
Measurement and Scaling Techniques-Errors in Measurement – Tests of Sound Measurement – Scaling and Scale Construction Techniques – Time Series Analysis – Interpolation and Extrapolation.
Data Collection Methods – Primary Data – Secondary data – Questionnaire Survey and Interviews.

UNIT III

Correlation and Regression Analysis – Method of Least Squares – Regression vs Correlation – Correlation vs Determination – Types of Correlations and Their Applications

UNIT IV

Statistical Inference: Tests of Hypothesis – Parametric vs Non-parametric Tests – Hypothesis Testing Procedure – Sampling Theory – Sampling Distribution – Chi-square Test – Analysis of variance and Co-variance – Multi-variate Analysis.

UNIT V

Report Writing and Professional Ethics: Interpretation of Data – Report Writing – Layout of a Research Paper – Techniques of Interpretation- Making Scientific Presentations in Conferences and Seminars – Professional Ethics in Research.

Text Books:

Research Methodology:Methods And Techniques – C.R.Kothari, 2nd Edition,New Age International Publishers.
Research Methodology: A Step By Step Guide For Beginners- Ranjit Kumar, Sage Publications (Available As Pdf On Internet)
Research Methodology And Statistical Tools – P.Narayana Reddy And G.V.R.K.Acharyulu, 1st Edition,Excel Books,New Delhi.

REFERENCES:

1. Scientists Must Write - Robert Barrass (Available As Pdf On Internet)
2. Crafting Your Research Future –Charles X. Ling And Quiang Yang (Available As Pdf On Internet)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech III semester (VLSI &ES) **L T P C**

4 0 0 4

(17D20302) HUMAN VALUES AND PROFESSIONAL ETHICS
(Elective V-OPEN ELECTIVE)

Unit I:
HUMAN VALUES:Morals, Values and Ethics-Integrity-Work Ethic-Service learning – Civic Virtue – Respect for others – Living Peacefully – Caring – Sharing – Honesty - Courage- Co Operation – Commitment – Empathy –Self Confidence Character – Spirituality.

Unit II:
ENGINEERING ETHICS: Senses of Engineering Ethics- Variety of moral issues – Types of inquiry – Moral dilemmas – Moral autonomy –Kohlberg‟s theory- Gilligan‟s theory- Consensus and controversy – Models of professional roles- Theories about right action- Self interest - Customs and religion –Uses of Ethical theories – Valuing time –Co operation – Commitment.

Unit III :
ENGINEERING AS SOCIAL EXPERIMENTATION: Engineering As Social Experimentation – Framing the problem – Determining the facts – Codes of Ethics – Clarifying Concepts – Application issues – Common Ground - General Principles – Utilitarian thinking respect for persons.

UNIT IV:
ENGINEERS RESPONSIBILITY FOR SAFETY AND RISK: Safety and risk – Assessment of safety and risk – Risk benefit analysis and reducing riskSafety and the Engineer- Designing for the safety- Intellectual Property rights(IPR).

UINIT V:
GLOBAL ISSUES: Globalization – Cross culture issues- Environmental Ethics – Computer Ethics – Computers as the instrument of Unethical behavior – Computers as the object of Unethical acts – Autonomous Computers- Computer codes of Ethics – Weapons Development - Ethics .

Text Books :

1. “Engineering Ethics includes Human Values” by M.Govindarajan, S.Natarajan and V.S.SenthilKumar-PHI Learning Pvt. Ltd-2009.
2. “Engineering Ethics” by Harris, Pritchard and Rabins, CENGAGE Learning, India Edition, 2009.
3. “Ethics in Engineering” by Mike W. Martin and Roland Schinzinger – Tata McGrawHill– 2003.
4. “Professional Ethics and Morals” by Prof.A.R.Aryasri, Dharanikota Suyodhana-Maruthi Publications.
5. “Professional Ethics and Human Values” by A.Alavudeen, R.Kalil Rahman and M.Jayakumaran , Laxmi Publications.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech III semester (VLSI &ES) **L T P C**

4 0 0 4

(17D20303) INTELLECTUAL PROPERTY RIGHTS
(Elective V-OPEN ELECTIVE)

UNIT – I

Introduction To Intellectual Property: Introduction, Types Of Intellectual Property, International Organizations, Agencies And Treaties, Importance Of Intellectual Property Rights.

UNIT – II

Trade Marks : Purpose And Function Of Trade Marks, Acquisition Of Trade Mark Rights, Protectable Matter, Selecting And Evaluating Trade Mark, Trade Mark Registration Processes.

UNIT – III

Law Of Copy Rights : Fundamental Of Copy Right Law, Originality Of Material, Rights Of Reproduction, Rights To Perform The Work Publicly, Copy Right Ownership Issues, Copy Right Registration, Notice Of Copy Right, International Copy Right Law.

Law Of Patents : Foundation Of Patent Law, Patent Searching Process, Ownership Rights And Transfer

UNIT – IV

Trade Secrets : Trade Secrete Law, Determination Of Trade Secrete Status, Liability For Misappropriations Of Trade Secrets, Protection For Submission, Trade Secrete Litigation.

Unfair Competition : Misappropriation Right Of Publicity, False Advertising.

UNIT – V

New Development Of Intellectual Property: New Developments In Trade Mark Law ; Copy Right Law, Patent Law, Intellectual Property Audits.

International Overview On Intellectual Property, International – Trade Mark Law, Copy Right Law, International Patent Law, International Development In Trade Secrets Law.

TEXT BOOKS & REFERENCES:

1. Intellectual Property Right, Deborah. E. Bouchoux, Cengage Learing.
2. Intellectual Property Right – Nleashmy The Knowledge Economy, Prabuddha Ganguli, Tate Mc Graw Hill Publishing Company Ltd.,